A study of integer sorting on multicores

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Abstract

Integer sorting on multicores and GPUs can be realized by a variety of approaches that include variants of distribution-based methods such as radix-sort, comparison-oriented algorithms such as deterministic regular sampling and random sampling parallel sorting, and network-based algorithms such as Batcher's bitonic sorting algorithm.

In this work we present an experimental study of integer sorting on multicore processors. We have implemented serial and parallel radix-sort for various radixes, deterministic regular oversampling and random oversampling parallel sorting, and also some previously little explored or unexplored variants of bitonic-sort and odd-even transposition sort.

The study uses multithreading and multiprocessing parallel programming libraries with the C language implementations working under Open MPI, MulticoreBSP, and BSPlib utilizing the same source code.

A secondary objective is to attempt to model the performance of these algorithm implementations under the MBSP (Multi-memory BSP) model. We first provide some general high-level observations on the performance of these implementations. If we can conclude anything is that accurate prediction of performance by taking into consideration architecture dependent features such as the structure and characteristics of multiple memory hierarchies is difficult and more often than not untenable. To some degree this is affected by the overhead imposed by the high-level library used in the programming effort. We can still draw however some reliable conclusions and reason about the performance of these implementations using the MBSP model, thus making MBSP useful and usable.

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1 Summary

Integer sorting on multicores and GPUs can be realized by traditional distribution-specific algorithms such as radix-sort [3, 12, 25, 28], or variants of it that use fewer rounds of the baseline count-sort implementation provided additional information about key values is available [6, 39]. Other approaches include algorithms that use specialized hardware or software features of a particular multicore architecture [4, 6, 22, 25]. Comparison-based algorithms have also been used with some obvious tweaks: use of deterministic regular sampling sorting [34] that utilizes serial radix-sort for local sorting [8, 9, 10] or use other methods for local sorting [38, 3, 5, 6, 22]. Network-based algorithms such as Batcher's [1] bitonic sorting [23, 3, 30, 31, 5] have also been utilized. In particualar, bitonic sorting is a low programming overhead algorithm and thus more suitable for GPU and few-core architectures, is simple to implement, and quite fast when few keys are to be sorted, even if its theoretical performance is suboptimal.

In this work we perform an experimental study of integer sorting on multicore processors using multithreading and multiprocessing based libraries that facilitate parallel programming. Our implementations need only recompilation of the same C language source to work under Open MPI [29], MulticoreBSP [36], and a multi-processing and out of maintenace library, BSPlib [19].

Towards this we have implemented (a) serial and parallel radix-sort for various radixes, named SR4 for the serial radix-256 version, PR4 for the parallel radix-256, and PR2 for the parallel radix-65536 versions, (b) previously little explored or unexplored variants of bitonic-sort named BTN, and odd-even transposition sort named OET respectively, (c) a variant of the random oversampling parallel sorting algorithm of [16] named GVR, (d) the deterministic regular oversampling parallel sorting algorithm of [13, 15] named GSD, and (e) a random oversampling parallel sorting algorithm named GER that differs from other random sample sorting approaches in that it follows instead the skeleton of deterministic regular sampling or oversampling methods [34, 13, 15].

We then present observations on a performance study of such algorithm implementations on multiple platforms and architectures and multiple programming libraries. If we can conclude anything is that precisely modeling their performance by taking into consideration architecture dependent features such as the structure and characteristics of multiple memory hierarchies is difficult and more often than not unusable or unreliable. This is primarily because of the uknown or difficult to model characteristics of the underlying software library that facilitates parallel programming. However we can still draw some very simple conclusions using traditional architecture independent parallel modeling under Valiant's BSP model [35] or the augmented MBSP model [17] that has recently been proposed by this author as a flat multi-memory extension of the BSP model for multicore or multimemory architectures. We have stayed away for example from Valiant's Multi-BSP model [37] for a variety of obvious reasons. Modern cache and memory hierarchies change from one processor generation to another that makes precise modeling of them a hopeless task. Writing portable code that is optimal under such conditions is next to impossible. The Multi-BSP hierarchical modeling is suitable for hierarchical algorithms. Implementing portable and efficient hierarchical algorithms is beyond the capabilities of this author, a hard task left to others, and frankly difficult if not impossible to achieve. Moreover, none of the algorithm implementations utilized in this study exhibits features of a hierarchical algorithm. In fact the GVR and GSD variants of [16] and [13, 15] respectively, purposefully eliminate hierarchical features of the original algorithms for the benefit of generating a portable and efficient and potentially performance predictable implementation. The hierarchical features inserted into [16, 13, 15] served only one purpose: to show theoretical optimality for extreme conditions when p, the number of processors is very close to n the number of keys to be sorted. It is for these reasons that we believe that the simplicity of MBSP is more suitable for modeling than Multi-BSP.

Some of the experimental conclusions drawn from this study are discussed briefly below. For small problem sizes (say n, the number of integer keys is lower than about 150,000 or so), BTN, the variant of bitonic sorting, indeed outperforms serial or parallel radix-sort with their more time-consuming setup, and complex communication/memory patterns for the core and thread count of the testbed platforms (up to 32 cores or hardware-supported threads). This has been observed indepependently by others before [3]. What has been quite even more extraordinary is that the variant OET of odd-even transposition sort implemented also exhibited good, yet slightly worse performance compared to BTN on some architectures. This did not use to be the case in the past when one had to deal with the p processors of a cluster, an SMP machine, or a supercomputer. It rather seems to be a featur of multicore architectures.

For small problem sizes, at around 16 cores or threads, GSD started consistently beating all variants of radix-sort and it was either better or had comparable performance to BTN. GER had a slightly worse performance than GSD yet it was also consistently better than all variants of radix-sort as well. GVR exhibited marginally worse performance than GER or GSD. This however might have to do with the different sampling methods and sample sizes used in GVR and GER and also in GSD. We shall study such behavior in another work.

For large problem sizes (say n is at least 8,000,000 or more), BTN and OET were in general uncompetitive. PR4 had an edge over the sampling based algorithms for large and increasing problem sizes, 32,000,000 to 128,000,000 but marginally only in most cases. PR2 had performance worse than BTN and OET in several cases. This is primarily a result of the high radix of PR2; more optimizations are needed for PR2 to become competitive.

Moreover, we have observed that assigning multiple threads per core is not recommended for CPUs with large number of cores. This is because of the additional demand to access a scarce resource, main memory (RAM), in data intensive applications that might also not be locality friendly. For CPUs with moderate number of cores, assigning multiple threads per core should never exceed the hardware supported bound (usually two), or be even lower than that. If the number of cores is small, multiple threads per core can be used as long as problem size is kept small, i.e. the application becomes less data intensive.

For parallel radix-sort of 32-bit integers, radix-2^8 radix-sorting i.e. four rounds of baseline count-sort is faster than the alternative radix-2^{16} sorting that uses two rounds. However, depending on the architecture and its structure of its caches (level-1, level-2 and level-3) it is possible that radix-2^{16} to outperform radix-2^8. This has not been observed in our experiments though.

Overall efficiency is dependent on the number of cores if the degree of parallelism is large. For degree of parallelism less than four or eight, efficiency can be expressed either in terms of number of cores or threads. As most architectures only support in hardware two threads per core, inefficiencies and significant drop in performance arise if one goes beyond that. For the multiprocessing library, BSPlib, exceeding the number of hardware cores leads to immediate drop in performance. In this latter case number of cores rather than number of threads determines or best describes speedup or efficiency.

2 Related work

The problem of sorting keys in parallel has been studied extensively. One major requirement in parallel algorithm design is the minimization of interprocessor communication that reduces non-computational overhead and thus speeds up parallel running time. In order to shorten communication several techniques are employed that allow coarse (eg. several consecutive keys at a time) rather than fine-grained (eg. few individual keys) communication. Coarse-grained communication usually takes advantage of locality of reference as well. Some of these optimizations work transparently in multicore or manycore programming as well. In parallel sorting, if one wants to sort n keys in parallel using p processors, one obvious way to achieve this is to somehow split the n keys into p sequences of approximately the same size and then sort these p sequences independently and in parallel using either the same algorithm recursively in a hierarchical fashion but in a serial setting, or resort to another fast serial algorithm, so that the concatenation (rather than merging) of the p sorted sequences generates the sorted output. For $p = 2$ this is quicksort [20].

The experimental work of [3] offers a collection of parallel algorithms that have been used unmodified or not as a basis for integer multicore or parallel sorting. One such algorithm has been radix-sort, another one has been sample-sort [33, 21, 32] i.e. random oversampling sorting along the lines of [32]. Key sampling employed in parallel sorting has been studied in [21, 32, 33] that provide algorithms with satisfactory and scalable theoretical performance. Using the technique of *random oversampling*, fully developed and refined in the context of parallel sorting [21, 33, 32], in order to sort n keys with p processors, one uses a sample of $ps - 1$ uniformly at random selected keys where s is the *random oversampling factor*. After sorting the sample of size $ps - 1$, one then identifies $p - 1$ splitters as equidistant keys in the sorted sample. Those $p - 1$ keys split the input into p sequences of approximately the same size that can then be sorted independently. In [32] it is shown that the p sequences of the n input keys induced by the $p - 1$ splitters will retain with high probability $O(n/p)$ keys each and will thus be balanced in size up to multiplicative constant factors if one regulates s properly. In [16], it is shown that by fine-tuning and carefully regulating this oversampling factor s, the p sequences have with high probability $(1 + \epsilon)n/p$ keys resulting in a finer balance. Parameter $0 < \epsilon < 1$ is a parameter that is controlled by s. The bounds on processor imbalance during sorting for [16] are tighter than those of any other random sampling or oversampling algorithm [21, 11, 32, 33].

Thus if one was to extend say a traditional quick-sort method to use oversampling, one would need to add more steps or phases to the sorting operation. These would include a sample selection phase, a sample-sort phase, a splitter selection phase, followed by a phase that splits the input keys around the chosen splitters. A subsequent routing operation of the split keys is followed by local sorting if possible or using the same algorithm recursively.

Algorithm GVR. The random oversampling algorithm in [16] follows this execution pattern. [16] generically indicates how one can sort the sample using algorithms from [27]. If $p^2 < n$, and it is so for the case of our multicore sorting study, one could perform sample sorting either serially or in parallel thus bypassing [27] methods. In our GVR adaptation of [16] we thus use bitonic-sort i.e. BTN for sample sorting. If one performs a binary search of the input keys to the $p-1$ splitters selected in random sampling the resulting communication would be rather fine-grained. There is a need to pack together all keys destined to the same processor. Thus in our implementation, following the binary search step we "count-sort" the keys based on the destination processor each one is destined to. This alas requires n/p extra space for the processor identifiers and n/p more space for the output of "count-sorting". At that point keys are ordered by destination into p sequences and then sequence i is dispatched to processor i. If this is not realized, fine-grain communication will degrade the performance of GVR. Furthermore, in the context of integer sorting the split keys are locally sorted using radix-sort i.e. SR4; there is no need for the recursion of [16].

Deterministic regular sampling as presented in [34] works as follows. First split regularly and evenly n input keys into p sequences of equal size (the first n/p or so keys become part of the first sequence, the next n/p keys part of the second and so on). Locally sort the p sequences independently (eg by using radix-sort if the keys are integer), and then pick from each sequence $p-1$ regular and equidistant sample keys for a sample of total size $p(p-1)$. A sorting (or multi-way merging) of these sample keys can be followed by the selection of $p-1$ equidistant splitters from the sorted sample. Those splitters are broadcast to all processors or cores, that then split their input keys around those $p-1$ splitters into p buckets. The keys of bucket i are routed to processor or core i in a follow-up communication step. The p received sequences by processor i, one per originating processor, are then merged using p-way merging and the algorithm terminates. One can then prove that if the n keys are split around the $p-1$ splitters, then none of the processors including processor i will receive more than $2n/p$ keys [34]. For this method to be optimal one needs to maintain $n/p > p^2$. The work of [8] also discusses the case of $n/p < p^2$.

Deterministic regular oversampling. In [13, 15, 14] the notion of regular sampling is extended to include oversampling thus giving rise to deterministic regular oversampling. In that context, $(p-1)s$ regular and equidistant sample keys are chosen from each one of the p sequences thus generating a larger sample of $p(p-1)s$ keys deterministically, with s being now the *regular oversampling factor*. One can claim [15] that each one of the p sequences split by the $p-1$ resulting splitters is of size no more than $(1+\delta)n/p$, where $\delta > 0$ also depends on the choice of s thus reducing a $2n/p$ imbalance into an $(1+\delta)n/p$ one with δ depending on s.

Algorithm GSD. In this study the algorithm of [15] is implemented quite faithfully including the parallel sample sorting step that involves the BTN implementation. The initial local sorting uses SR4 [7]. More details follow in the next section.

Algorithm GER. Random oversampling-based sorting is supposed to be superior to deterministic regular sampling or oversampling-based sorting as the regular oversampling factor s can not be finely-tuned as much as the random oversampling factor s [13, 15]. Moreover the deterministic algorithms suffer from the final multi-way merging step. To test this, in this study we also implement a second random oversampling parallel sorting algorithm, GER, that works however quite differently from GVR and other random sampling algorithms and its skeleton draws from deterministic regular sampling [34] or regular oversampling [13, 15] i.e. it is very similar to GSD. In such an approach local key sorting comes first before sample and splitter selection, followed at the very end by a multi-way merging that is less locality-sensitive. Thus the only difference between GER and GSD is the sample selection step: the former's one resembles that of GVR's. For both cases however BTN is used for sample sorting. More details follow in the next section.

The algorithm of [34] was used by [8] in the context of integer sorting; initial local sorting involved radix-sort. Subsequently [9, 10] utilized this approach for GPU sorting of arbitrary (not necessarily integer) keys. Similarly to the approach of [13, 15] but differently, a sample of size ps is being used rather than the $p(p-1)s$ of [13, 15]. The GPU architecture's block thread size determines p and other GPU constraints dictate s. Thus effectively the implied oversampling factor of [13, 15] becomes $s/(p-1)$ in [9, 10]. [30] also performs GPU sorting by using a bitonic sorting method. The conclusions of the two papers [30, 9] agree that bitonic-sorting works better for small values of n and sample sort [9, 10] or radix-sort [30] is better for larger n. Their overall conclusions are in line with those of [3].

In [38] a parallel merge-sort is analyzed and implemented on multicores. The parallelization of merge-sort is not optimal. An $(n/p)\lg(n/p)$ local and independent sorting on p threads/cores is followed by a merging yielding a speedup bounded by $n\lg(n)/(n\lg(n)/p+2n)$. This work is similar to that of [39]. The latter deals with multisets (keys taking a range of distinct values). Even on four processing cores efficiency is less than 50%. [4] utilizes a quicksort approach and AVX-512 instructions on Intel's Knights Landing. For small problem sizes the use of insertion sort is replaced by bitonic sort to allow for vectorization. This is close to the work of [5] that introduces GPU-Quicksort. The thread processors perform a single task: determining whether a key is smaller or not than a splitter. Then a rearranging of the keys is issued following something akin to a scan/parallel prefix [26] operation. Its performance is compared to a radix-sort implementation and shown to be slightly better but mostly worse than a Hybridsort approach that uses bucketsort and merge-sort (whose performance depends on the distribution of the input keys).

A third algorithm used in the pioneering work of [3] is bitonic sorting. For sorting n keys (integer or otherwise) the bitonic sort of [3] employs a $\Theta(\lg^2(n))$ stage bitonic sort. If the input is regularly partitioned, n/p keys are located inside a single processor. Thus bitonic merging of those keys can be done entirely within the corresponding processor's memory as observed in [3]; the authors alternatively proposed using linear-time serial merging over the slower bitonic merging. It is worth noting that the bitonic sort of [3] for small n outperformed the other sorting methods as implemented on a Connection Machine CM-2. This is due to the low programming overhead of the method as also highlighted in the previous section. This approach of [3] to bitonic sorting has been followed since then. More recently [31] is using an implementation drawn from [23] for bitonic sorting on GPUs and CPUs. Such an implementation resembles the one above where for n/p keys local in-core operations are involved. Alas, overall GPU performance is rather unimpressive: a 10x speedup over the CPU implementation on an NVIDIA GT520, or 17x on a Tesla K40C for 5M keys, and a modest 2-3x speedup for fewer keys.

However neither [3] nor the other implementations of bitonic sort cited [31, 23] or to be cited later in this section considered that bitonic sorting involving n keys on p processors/ cores/ threads can utilize a bitonic network of $\Theta(\lg^2(p))$ stages. If p is substantially smaller than n, then the savings are obvious compared to a $\Theta(\lg^2(n))$ stage bitonic sorter utilized in [3, 31, 23] and other works.

Algorithm BTN. Indeed this author [13, 15] highlighted the possibility and used $\Theta(\lg^2(p))$ stage bitonic sorting for sample sorting involving more than p keys in the context of bulk-synchronous parallel [35] sorting. In particular, [13, 15] cite the work of [2, 24] for first observing that a p-processor bitonic sorter can sort n keys in $\lg(p)(\lg(p)+1)/2$ stages (or rounds). Think of sorting with this p-processor bitonic sorter p 'keys' where each 'key' is a sorted sequence of n/p regular keys. A comparison of two 'keys' on two processors gets resolved by merging the two n/p sorted sequences located to these two processors and then assigning the lower half, the smaller keys, to the lower indexed (eg. left processor) and the upper half to the higher indexed processor (eg. right processor). At start-up before bitonic sorting commences each one of the p 'keys' needs to be in the right order i.e. the n/p keys of each processor are locally sorted. This local sorting can utilized merge-sort or if the keys are integer radix-sort, or something else. In our realization of this $\lg(p)(\lg(p)+1)/2$ stage bitonic sorter, local initial sorting is realized by SR4. We have been calling this implementation BTN.

Algorithm OET. Odd-even transposition sort [26] is an unrefined version of bubble-sort that has been used for sorting in array structured parallel architectures (one-dimensional arrays, two-dimensional meshes, etc). In such a sort n keys can be sorted by n processors in n rounds using an oblivious sorting algorithm. In an odd-indexed round a key at an odd-indexed position is compared to the even-indexed key to its immediate right (index one more); a swap is performed if the former key is greater. Like-wise for an even-indexed round. A very simple observation we make is that if the number of processors/cores is p, then a p-wide p-round odd-even transposition sort can sort n keys by dealing with n/p key sequences, one such sequence per processor as it was done in the case of BTN above. Each one of the p cores is assigned one 'key', a sorted sequence of n/p regular keys. Comparisons between 'keys' get resolved the same way as in BTN by merging the two sorted sequences of the two 'keys' involving n/p regular keys each. Then the smaller n/p keys get separated from the larger n/p keys; the former are destined to the lower-indexed, and the latter to the next-indexed processor respectively. Likewise as before, at start-up the p 'keys' must be sorted before the p-wide odd-even transposition sort commences its execution on the n key input. This is a local sort operation. We call this p-wide implementation of odd-even transposition sort used to sort n keys OET for future references; local initial sorting utilizes SR4 [7].

The implementation of AA-sort is undertaken in [22]. AA-sort can be thought of as a bubble-sort like enhancement of the odd-even transposition sort we discussed earlier and called OET. Whereas in OET we have odd and even phases in AA-sort there is no such distinction and either a bubble-sort step (from left to right) is executed if a gap parameter g has a value of 1, or non-adjacent keys are bubble-sorted if g is greater than 1. (Thus $a[i]$ and $a[i+g]$ are then compared.) Likewise to OET initially each n/p sequence is sorted; in the case of AA-sort, a merge-sort is used. The use of a bubble-sort oriented approach is to exploit vectorization instructions of the specific target platforms: PowerPC 970MP and Cell Broadband Engine(BE). In the implementations [22] present also results for a bitonic sort based implementation. AA-sort seems to be slightly faster than bitonic sort with SIMD enhancements for 16K random integers. In the Cell BE, AA-sort outperforms bitonic sort for 32M integers (12.2 speedup for the former over 7.1 for the latter on 16 CELL BE cores).

The AQsort algorithm of [25] utilizes quicksort, a comparison-based sorting algorithm, and OpenMP is utilized to provide a parallel/multithread version of quicksort. Though its discussion in an otherwise integer sorting oriented works as this one might not make sense, there are some interesting remarks made in [25] that are applicable to this work. It is observed that hyperthreading provides no benefit and that for Intel and AMD CPUs best performance is obtained for assigning one thread per core. For Intel Phi and IBM BG/Q two threads per core provide marginally lower running times even if four threads are hardware supported.

In [28] radix-sort is discussed in the context of reducing the number of rounds of count-sort inside radix-sort by inspecting key values' most significant bits. A parallelized radix-sort along those lines achieves efficiencies of approximately 15-30% (speedup of 5-10 on 32 cores). Other conclusions are in line with [25] in that memory channels can't keep up with the work assigned from many parallel threads.

3 Implementations

3.1 MBSP model

In this section we shall describe the algorithms that we shall implement and analyze their performance under the *Multi-memory Bulk-Synchronous Parallel (MBSP)* model of computation [17]. The MBSP is parameterized by the septuplet (p, l, g, m, L, G, M) to abstract, computation and memory interactions among multi-cores. In addition to the modeling offered by the BSP model [35] and abstracted by the triplet (p, l, g), the collection of core/processor components has m alternative memory units distributed in an arbitrary way, and the size of the "fast memory" is M words of information. The cost of memory unit-related I/O is modeled by the pair (L, G). L and G are similar to the BSP parameters l and g respectively. Parameter G expresses the unit transfer time per word of information and thus reflects the memory-unit throughput cost of writing a word of information into a memory unit (i.e. number of local computational operations as units of time per word read/written). Parameter L abstracts the memory-unit access latency time that reflects access delays contributed mainly but not exclusively by two factors: (a) unit access-related delays that can not be hidden or amortized by G, and (b) possible communication-related costs involved in accessing a non-local unit as this could require intraprocessor or interprocessor communication.

Using the MBSP cost modeling generic cache performance will be abstracted by the pair (L, G). Parameter m would be set to p and M will be ignored; we will assume that M is large enough to accommodate the radix-related information of radix-sort. Intercore communication will be abstracted by (p, l, g). Since such communication is done through main memory, g would be the cost of accessing such memory (aka RAM). We shall also ignore l and L. This is possible because in integer-sorting the operations performed are primitive and interaction with memory is the dominant operation. Thus the cost model of an algorithm would abstract only cost of access to the fast memory (G) and cost of access to the slow memory (g). Then we will use the easy to handle $g = 5G$ to further simplify our derivations. This is based on the rather primitive thinking that $20ns$ and $100ns$ reflect access times to a cache (L2 or higher) and main memory respectively thus defining a ratio of five between them.

3.2 SR4, PR2, PR4, BTN and OET under MBSP

Serial radix-r radix-sort: SR4

A serial radix-sort (previously called SR4) is implemented and used for local independent sorting in the odd-even transposition sort and bitonic sort implementations. The radix used is $r = 256$ i.e. it is a four-round count-sort. In each round of count-sort the input is read twice, first during the initial counting process and last when the output is to be generated, and the output is generated once. Thus the cost of such memory accesses is $3Ng$, with g referring to the cost of accessing the main memory and accounts for two input and one output operation. Moreoever allocation and initialization of the count array incurs a cost of $2rG$, with G being the cost of accessing the fast cache memory. We shall ignore this cost that is dominated by other terms. During the count operation the count array is accessed N times and so is during the output operation for a total cost of $2NG$. Thus the overall cost of a round is $3Ng + 2NG$. For all four rounds of 32-bit sorting the total cost is given by the following.

$$T_s(N, g, G, r) \quad = \quad (32/\lg(r)) \cdot (3Ng + 2NG)$$

If $g = 5G$ and $r = 256$ then

$$T_s(N, G) = 68NG \tag{1}$$

Parallel radix-r radix-sort: PR4 and PR2

We shall denote with PR2 and PR4 radix $r = 2^{16}$ and $r = 2^8$ parallel radix-sort algorithms. Ignoring some details that are implementation dependent such as the use of counters in the serial part and local and remote copies used in the parallel part, we recognize a cost $2rpg$ due to scatter and gather operations involved in the parallel part the algorithm. If n keys are to be sorted, each processor or core is assigned roughly $N = n/p$ keys. A $2NG$ cost is assigned for the same reasons that was assigned in the serial version. A $3Ng$ of the serial version will become $4Ng$ to account for a communication required before the output array is formed in a given round of count-sort.

$$T_p(N, g, G, p, r) \quad = \quad (32/\lg(r)) \cdot (4Ng + 2NG + 2prg)$$

If $g = 5G$ and $r = 256$ then

$$T_p(n, G, p) = (88n/p + 40 \cdot 256 \cdot p)\, G \tag{2}$$

If $g = 5G$ and $r = 256^2$ then

$$T_p(n, G, p) = \left(44n/p + 20 \cdot 256^2 \cdot p\right) G \tag{3}$$

Odd-even transposition sort: OET

We analyze the algorithm previously referred to as OET. If n keys are to be sorted, each processor or core is assigned roughly $N = n/p$ keys. First the N keys per processor or core are sorted using a radix $r = 256$ radix-sort independently and in parallel of each other that requires time $T_s(n/p, G)$. Then a p round odd-even transposition sort takes place utilizing n/p sorted sequences as explained earlier for OET. One round of it requires roughly $4Ng$ for communication and merging (two input and one output arrays). Thus the overall cost of all p phases of OET will be as follows.

$$T_o(n, g, G, p) \quad = \quad T_s(n/p, G) + p\,(4n/p)\, g$$

If $g = 5G$ and $r = 256$ then

$$T_o(n, G, p) = (68n/p + 20n)\, G \tag{4}$$

Bitonic Sort: BTN

We analyze the algorithm previously referred to as BTN. If n keys are to be sorted, each processor or core is assigned roughly $N = n/p$ keys. First the N keys per processor or core are sorted using a radix $r = 256$ radix-sort independently and in parallel of each other that requires time $T_s(n/p, G)$. Then $\lg(p)(\lg(p) + 1)/2$ stages of a p-processor bitonic-sort are realized as explained in Section 2. One round of it requires roughly $4Ng$ for communication and merging/comparing (two input and one output arrays). Thus the overall cost of all stages of bitonic sort will be as follows.

$$T_b(n, g, G, p) \quad = \quad T_s(n/p, G) + (\lg(p) \cdot (\lg(p) + 1)/2) \cdot (4n/p)\, g$$

If $g = 5G$ and $r = 256$ then

$$T_b(n, G, p) = (68n/p + (10n \lg(p)(\lg(p) + 1))\,/p)\, G \tag{5}$$

3.3 Oversampling algorithms: GSD, GVR, GER

GSD is depicted in Algorithm 1. Within GSD parameter s is the regular oversampling factor whose value is regulated through the choice of $r = \omega_n$. Parameter $r = \omega_n$ could have been included in the parameter list of GSD. The theorem and proof that follow simplify the proof and the results shown in a more general context in [13, 15].

Algorithm 1 GSD (X, n, p) {sorts n integer keys of X }

1: LOCALSORTING. The n input keys are regularly and evenly split into p sequences each one of size approximately n/p. Each sequence is sorted by SR4. Let X_k, $0 \le k \le p-1$, be the k-th sequence after sorting.

2: SAMPLE SELECTION. Let $r = \lceil \omega_n \rceil$ and $s = rp$. Form locally a sample T_k from the sorted X_k. The sample consists of $rp-1$ evenly spaced keys of X_k that partition it into rp evenly sized segments; append the maximum of the sorted X_k (i.e. the last key) into T_k so that the latter gets rp keys. Merge, in fact sort, all T_k into a sorted sequence T of rp^2 keys using BTN.

3: SPLITTER SELECTION. Form the splitter sequence S that contains the $(i \cdot s)$-th smallest keys of T, $1 \le i \le p-1$, where $s = rp$. Broadcast splitters.

4: SPLIT INPUT KEYS. Split the sorted X_k around S into sorted subsequences $X_{k,j}$, $0 \le j \le p-1$, for all $0 \le k \le p-1$ using binary search. Processor k sends to processor j sequence $X_{k,j}$.

5: MERGING. Subsequences $X_{k,j}$ for all $0 \le k \le p-1$ are merged into Y_j, for all $0 \le j \le p-1$ using p-way merging. The concatenation Y of all Y_j is returned.

Theorem 1 *For any n and $p \le n$, and any function ω_n of n such that $\omega_n = \Omega(1)$, $\omega_n = O(\lg n)$ and $p^2 \omega_n^2 \lg^2 n = o(n)$, operation GSD requires time at least $T_s(n/p, G) + 5Gn_{max} \lg p$, plus low order terms that are $o(T_s(n/p, G))$, where $n_{max} = (1 + 1/\lceil \omega_n \rceil)(n/p) + \lceil \omega_n \rceil p$.*

Proof: The input sequence is split arbitrarily into p sequences of about the same size (plus or minus one key). This is step 1 of GSD. Parameter r determines the desired upper bound in key imbalance of the p sorted sequences Y_k that will form the output. The term $1 + 1/r = 1 + 1/\lceil \omega_n \rceil$ that will characterize such an imbalance is also referred to as *bucket expansion* in sampling based randomized sorting algorithms [3]. In the discussion to follow we track constant values for key sorting and multi-way merging but use asymptotic notation for other low-order term operations. In step 1, each one of the p sequences is sorted independently of each other using SR4. As each such sequence is of size at most $\lceil n/p \rceil$, this step requires time $T_s(n/p, G)$.

Subsequently, within each sorted subsequence X_k, $\lceil \omega_n \rceil p - 1 = rp - 1$ evenly spaced sample keys are selected, that partition the corresponding sequence into rp evenly sized segments. Additionally, the largest key of each sequence is appended to T_k. Let $s = rp$ be the size of the so identified sequence T_k. Step 2 requires time $O(s)g$ to perform. The p sorted sample sequences, each consisting of $s = rp$ sample keys, are then merged/sorted using BTN in time $T_b(rp^2, G, p)$ into T. Let sequence $T = \langle t_1, t_2, \ldots, t_{ps} \rangle$ be the result of that operation. In step 3, a sequence S of evenly spaced splitters is formed from the sorted sample by picking as splitters keys t_{is}, $1 \leq i < p$. This step takes time $O(p)g$. Step 4 splits X_k around the sample keys in S. Each one of the p sorted sequences decides the position of every key it holds with respect to the $p-1$ splitters by way of serial merging the $p-1$ splitters of S with the input keys of X_k in $p - 1 + n/p$ time per sequence. Alternately this can be achieved by performing a binary search of the splitters into the sorted keys in time $p \lg (n/p)$, and subsequently counting the number of keys that fall into each one of the p so identified subsequences induced by the $p - 1$ splitters. The overall running time of this step is $p \lg (n/p) g$ if binary search is performed.

In step 4, $X_{k,j}$ is the j-th sorted subsequence of X_k induced by S. This subsequence will become part of the Y_j-th output sequence in step 5. In step 5, p output sequences Y_j are formed that will eventually be concatenated. Each such output sequence Y_j is formed from the at most p sorted subsequences $X_{k,j}$ for all k, formed in step 4. When this step is executed, by way of Lemma 1 to be shown next, each Y_j will comprise of at most $p = \min\{p, n_{max}\}$ sorted subsequences $X_{k,j}$ for a total of at most n_{max} keys for Y_j, and n keys for Y, where $n_{max} = (1 + 1/\lceil \omega_n \rceil)(n/p) + \lceil \omega_n \rceil p$. The cost of this step is that of multi-way merging i.e. $n_{max} \lg pg$.

LocalSorting and Merging thus contribute $T_s(n/p, G) + n_{max} \lg pg$, noting $g = 5G$. Sample selection and sample-sorting contributions amount to $T_b(rp^2, G, p)$. Other contributions such as $O(pG)$ of step 3 and $5p \lg (n/p) G$ can be ignored. ■

It remains to show that at the completion of step 4 the input keys are partitioned into (almost) evenly sized subsequences. The main result is summarized in the following lemma.

Lemma 1 *The maximum number of keys n_{max} per output sequence Y_j in GSD is given by* $(1 + 1/\lceil \omega_n \rceil)(n/p) + \lceil \omega_n \rceil p$, *for any ω_n such that $\omega_n = \Omega(1)$ and $\omega_n = O(\lg n)$, provided that $\omega_n^2 p = O(n/p)$ is also satisfied.*

Proof: Although it is not explicitly mentioned in the description of algorithm GSD we may assume that we initially pad the input so that each sequence has exactly $\lceil n/p \rceil$ keys. At most one key is added to each sequence (the maximum key can be such a choice). Before performing the sample selection operation, we also pad the input so that afterwards, all segments have the same number of keys that is, $x = \lceil \lceil n/p \rceil / s \rceil$. The padding operation requires time at most $O(s)$, which is within the lower order terms of the analysis of Theorem 1, and therefore, does not affect the asymptotic complexity of the algorithm. We note that padding operations introduce duplicate keys; a discussion of duplicate handling follows this proof.

Consider an arbitrary splitter t_{is}, where $1 \leq i < p$. There are at least isx keys which are not larger than s_{is}, since there are is segments each of size x whose keys are not larger than s_{is}. Likewise, there are at least $(ps - is - p + 1)x$ keys which are not smaller than s_{is}, since there are $ps - is - p + 1$ segments each of size x whose keys are not smaller than s_{is}. Thus, by noting that the total number of keys has been increased (by way of padding operations) from n to psx, the number of keys b_i that are smaller than s_{is} is bounded as follows.

$$isx \leq b_i \leq psx - (ps - is - p + 1)\, x.$$

A similar bound can be obtained for b_{i+1}. Substituting $s = \lceil \omega_n \rceil p$ we therefore conclude the following.

$$b_{i+1} - b_i \leq sx + px - x \leq sx + px = \lceil \omega_n \rceil px + px.$$

The difference $n_i = b_{i+1} - b_i$ is independent of i and gives the maximum number of keys per split sequence. Considering that $x \leq (n + ps)/(ps)$ and substituting $s = \lceil \omega_n \rceil p$, the following bound is derived.

$$n_{max} = \left(1 + \frac{1}{\lceil \omega_n \rceil}\right) \frac{n + ps}{p}.$$

By substituting in the numerator of the previous expression $s = \lceil \omega_n \rceil p$, we conclude that the maximum number of keys n_{max} per output sequence of GSD is bounded above as follows.

$$n_{max} = \left(1 + \frac{1}{\lceil \omega_n \rceil}\right) \frac{n}{p} + \lceil \omega_n \rceil p.$$

The lemma follows. ■

The skeleton of GSD is being used in developing GER. Random oversampling-based algorithms in the traditional approach of [21, 33, 32, 16] do not involve a LocalSorting first step that distinguishes GER from other random oversampling approaches. For reference, we also outline GVR next.

Algorithm 2 GER (X, n, p) {sorts n integer keys of X }

1: LocalSorting. The n input keys are regularly and evenly split into p sequences each one of size approximately n/p. Each sequence is sorted by SR4. Let X_k, $0 \le k \le p-1$, be the k-th sequence after sorting.

2: Sample Selection. Let $s = 2\omega_n^2 \lg n$. Form a sample T from the corresponding X_k. The sample consists of $sp - 1$ keys selected uniformly at random from the keys of all X_k. Sort T using BTN.

3: Splitter Selection. Form the splitter sequence S that contains the $(i \cdot s)$-th smallest keys of T, $1 \le i \le p-1$.

4: Split input keys. Split the sorted X_k around S into sorted subsequences $X_{k,j}$, $0 \le j \le p-1$, for all $0 \le k \le p-1$. Processor k sends to processor j sequence $X_{k,j}$.

5: Merging. Subsequences $X_{k,j}$ for all $0 \le k \le p-1$ are merged into Y_j, for all $0 \le j \le p-1$. The concatenation Y of Y_j is returned.

Although partitioning and oversampling in the context of sorting are well established techniques [21, 33, 32], the analysis in [16] summarized in Lemma 2 below allows one to quantify precisely the key imbalance of the output sequences Y_j. Let $X = \langle x_1, x_2, \ldots, x_n \rangle$ be an ordered sequence of keys indexed such that $x_i < x_{i+1}$, for all $1 \le i \le n-1$. The implicit assumption is that keys are unique. Let $Y = \{y_1, y_2, \ldots, y_{ps-1}\}$ be a randomly chosen subset of $ps - 1 \le n$ keys of X also indexed such that $y_i < y_{i+1}$, for all $1 \le i \le ps-2$, for some positive integers p and s. Having randomly selected

Algorithm 3 GVR (X, n, p) {sorts n integer keys of X }

1: SAMPLE SELECTION. The n input keys are regularly and evenly split into p sequences each one of size approximately n/p. Let X_k, $0 \le k \le p-1$, be the k-th sequence. Let $s = 2\omega_n^2 \lg n$. Form a sample T from the corresponding X_k. The sample consists of $sp - 1$ keys selected uniformly at random from the keys of all X_k. Sort T using BTN.

2: SPLITTER SELECTION. Form the splitter sequence S that contains the $(i \cdot s)$-th smallest keys of T, $1 \le i \le p - 1$.

3: SPLIT INPUT KEYS. Split X_k around S into unordered subsequences $X_{k,j}$, $0 \le j \le p - 1$, for all $0 \le k \le p - 1$. This requires a binary search of X_k into S followed by a count-sort oriented approach that sorts the keys of X_k with respect to the processor index j they are destined to thus determining the corresponding $X_{k,j}$ subsequence. Then and only then does the key moves to $X_{k,j}$. Processor k sends to processor j sequence $X_{k,j}$.

4: LOCALSORTING. Subsequences $X_{k,j}$ for all $0 \le k \le p - 1$ are concatenated into Y_j, for all $0 \le j \le p - 1$. Then Y_j is sorted locally on processor j using SR4. The concatenation Y of the sorted Y_j is returned.

set Y, a partitioning of $X - Y$ into p subsets, $X_0, X_1, \ldots, X_{p-1}$ takes place. The following result shown in [16] is independent of the distribution of the input keys.

Lemma 2 *Let $p \geq 2$, $s \geq 1$, $ps < n/2$, $n \geq 1$, $0 < \varepsilon < 1$, $\rho > 0$, and*

$$s \geq \frac{1+\varepsilon}{\varepsilon^2}\left(2\rho \log n + \log\left(2\pi p^2 (ps-1) e^{1/(3(ps-1))}\right)\right).$$

Then the probability that any one of the X_i, for all i, $0 \leq i \leq p-1$, is of size more than $\lceil (1+\varepsilon)(n-p+1)/p \rceil$ is at most $n^{-\rho}$.

To conclude, the analysis of Theorem 1 is applicable to GER. For GVR, the choice of s in step 1 of Algorithm 3 guarantees with high probability that no processor receives in step 4 more than $n_{max} = (1 + 1/\omega_n)(n/p)$ keys. Thus whereas local sorting in GSD and GER involved the same number of keys per processor (plus or minus one) and multi-way merging in step 5 was unbalanced, in the case of GVR binary search over the splitters is quite balanced and the last step 4 involving local sorting is unbalanced. Therefore we have the following.

Theorem 2 *For any n and $p \leq n$, and any function ω_n of n such that $\omega_n = \Omega(1)$ and $p^2 \omega_n^2 \lg^2 n = o(n)$, operation GER requires time at least $T_s(n_{max}, G) + 5G(n/p)\lg p$, plus low order terms that are $o(T_s(n/p, G))$, where now $n_{max} = (1 + 1/\omega_n)(n/p)$.*

4 Experiments

All implementations undertaken in this work are in ANSI C; the same code need only be recompiled but does not need to be rewritten to work with three parallel, multiprocessing or multithreaded programming libraries: OpenMPI [29], MulticoreBSP [36], and BSPlib [19]. The source code is available through the author's web-page [18]. CONFIG1 was a 2-processor Intel Xeon E5-2660 v2 with 256GiB of memory providing a total of 20 cores and 40 threads. CONFIG2 an 8-processor quad-core AMD Opteron 8384 Scientific Linux 7 workstation with 128GiB of memory providing a total of 32 cores/threads. CONFIG3 was a 2-processor Intel Xeon E5-2630 v4 with 256GiB of memory providing a total of 20 cores and 40 threads. CONFIG4 was an Intel Xeon E3-1245 v6 with 32GiB of memory providing a total of 4 cores and 8 threads.

The version of OpenMPI available and used is 1.8.4. The version of OpenMPI used is 1.8.1. Version 1.2.0 of MulticoreBSP is used and version 1.4 of BSPlib. The source code is compiled using the native gcc compiler `gcc version 7.3.0` with optimization options `-O3 -march=native` and `-ffast-math -funroll-loops` and using otherwise the default compiler and library installation.

Indicated timing results (wall-clock time in seconds) in the tables to follow are the averages of four experiments. We used modest problem sizes of $8192 \times 10^3, 32768 \times 10^3, 131072 \times 10^3$ integers. We shall refer to them in the remainder as 8M, 32M, and 128M but we caution what this means for the corresponding values ($1M = 1024000$). This is the total problem size, not the per processor size. We have also run some experiments for smaller problem sizes on CONFIG3 ranging from 8192 up to 131072 keys over all cores/threads. Parameter p indicates the number of threads, cores or processes utilized. For CONFIG1 - CONFIG3 we used $p = 4, 8, 16, 32$ and for CONFIG4 $p = 2, 4, 8$. For the serial algorithm SR4 we report wall clock time. For the other algorithms i.e. PR4, PR2, BTN, OET, GSD, GVR and GER we only report speed up figures obtained from wall clock time and the corresponding p. We first provide a summary of the results for the four configurations. Then we list a set of observations that we have drawn from this experimental study.

For CONFIG1, a clear winner is PR4 for large n and p. The maximum observed speedup was close to the number of physical cores (speedup 16.58 for 20 cores) and when the number of threads was equal to the maximum of 2 threads per cores ($p = 32$ threads). The absolute maximum speedup was observed for BSPlib closely followed by MulticoreBSP and openMPI. It is quite surprising that an out of maintenance library that uses multiprocessing can still perform at high level. The latter had worse results for 8M sizes relative to the other two libraries. PR2 was very slow across all libraries exhibiting better performance under MulticoreBSP and worse under BSPlib. Bitonic sort BTN had its best performance for $p = 16$ or $p = 32$ for BSPlib but it was still twice or thrice slower than PR4. Nothing unexpected with OET. The three oversampling algorithms were slower than PR4 by roughly 25% but were competitive and close to even for smaller problem size 8M and 32M. GSD and GER had the drawback of multi-way merging which is currently very unoptimized in our implementation. GVR and GER had also to deal with calling random(). Moreover GVR needed an extra step to avoid fine grain communication; all keys destined to a single processor were packed together.

For CONFIG2, an older AMD architecture things changed. GVR primarily was the leader under OpeMPI, followed by MulticoreBSP and then BSPlib. The maximum achieved speedup was a lower 9.69. PR2 continued its slump under OpenMPI and BSPlib but outperformed PR4 in MulticoreBSP. Under OpenMPI PR4 and GSD and GER had roughly the same performance for 128M with an advantage to PR4, but for 8M and 32M all of GSD and GER and of course GVR performed better. For MulticoreBSP, PR4 was better than GSD and GER for the largest size 128M only. BSPlib extracted better performance from the oversampling methods than PR4. BTN and OET had miserable performance. The 8 CPUs of the AMD configuration is probably the reason for that. Even if this configuration had 32 cores (32 threads) vs 20 cores (and 40 threads) of CONFIG1, the maximum speed up observed and thus efficiency was lower at 9.69 out of 32 vs 16.58 out of 20 for CONFIG1.

For CONFIG3, a more recent architecture the maximum speedup was only 11.86 for PR4 under OpenMPI. PR4 had the best overall performance across all libraries. Under OpenMPI all of PR4, GSD, GVR, GER exhibited maximum performance as well. The latter three algorithms were only 10% or less off than PR4 and had better performance for small problem sizes.

CONFIG4 is a universally bad platform across all libraries and algorithms. With 4 cores and 8 hardware supported threads, the maximum speed up observed was an 1.83 for 32M. We can't explain such a result given the performance of the other three configurations.

Observation 1: Thread size per core. For the AMD platform CONFIG2 one thread per core is a requirement for extracting best performance. This is in accordance to remarks by [25] and [28]. For the Intel configurations CONFIG1 and CONFIG3 the hardware thread support utilization was an absolute maximum to extract maximum performance; in our experiments we used 32 out of a possible 40 threads on 20 cores. Experiments for $p = 64$ that use more than two threads per core were slow and inefficient.

Observation 2: Hyperthreading. For the Intel CONFIG1 and CONFIG3 two threads per core is a requirement for extracting consistently better performance thus deviating from [25]. Thus the one thread per core recommendation or observation of [25] might not be current any more for more recent architectures.

Observation 3: Libraries. OpenMPI's library latency makes it perform better in larger problem sizes than MulticoreBSP and BSPlib. BSPlib with its multiprocessing only support but low library overhead is extremely competitive and several times more efficient than OpenMPI, despite its age and non support. It is possible to extract better performance out of it, if one experiments with is communication parameters and their defaults.

Observation 4: 4-round vs 2-round radix-sort. Across the board PR4 is better than PR2. This is because of the radix r and the way our implementation handles the routing of radix $r = 256$ and $r = 65536$ sorting. One may need to optimize PR2 if it is and can become competitive to PR4.

Observation 5: MBSP modeling SR4 vs PR4. We may use equation 1 and equation 2 to determine the relative efficiency of a parallel four-round radix-sort. We have then than

$$T_s(n, G)/T_p(n/p, G, p) \quad = \quad 68nG/\left(88n/p + 40 \cdot 256 \cdot p\right) G$$

The fraction for large n is approximately $68p/88 \approx 0.77p$. Thus for $p = 4, 8, 16$ we should not be anticipating speedups higher than about $3, 6$ and 12 respectively for CONFIG1. Indeed this is the case if we consult Table 1 and also Table 3. It is also the case for Table 2 though the speedup values there are much less. This might mean that the assumption $g = 5G$ might not be accurate. But it offers a very rough initial estimation of what one should expect. Note also that the ratio g/G is not constant; large problem sizes are slow memory bound vs smaller problem sizes.

Observation 6: MBSP modeling SR4 vs GSD. The ratio of equation 1 and the expression for the running time of GSD as derived from Theorem 1 which is $T_s(n/p, G) + 5Gn_{max} \lg p$, is approximately

$$T_s(n, G)/(T_s(n/p, G) + 6Gn \lg p/p) \approx (68 \cdot p) / (68 + 6 \cdot \lg(p))$$

This is because for $n < 128,000,000$, $n_{max} \leq 1.2n$ for $\omega_n = \lg(\lg n)$ or so. For $p = 4, 8, 16$ we should be expecting speedup figures in the range of $3.4, 6.3$, and 11.82 respectively. Indeed this is the case as one can deduce from Table 1 - Table 3. The highest speedup observed for the corresponding processor/thread sizes is, according to Table 1 in the range $2.6 - 3.16$ for $p = 2$, in the range $4.44 - 5.31$ for $p = 4$, and the range $6.15 - 8.50$ for $p = 16$. Note that the denominator of the fraction above should also include asymptotically smaller terms as explained in the analysis of Theorem 1. An asymptotically small term might be significant for small values of n or p.

Note that under Observations 5 and 6 we did not consider the case for $p = 32$. This is because for say CONFIG1 with 20 cores, a $p = 32$ implies that multiple threads (two) are assigned to some of the cores. There is a non-homogeneity that any modelling with MBSP or any other model cannot reliably capture. Moreover the ratio g/G is also expected to be non-constant either.

Observation 7: Smaller problem size sorting. Table 5 presents timing results (in microseconds) for small problem sizes for selected algorithms. The low overhead BTN fares better than PR4 or SR4 and more often than not also fares better than GSD. It is hard to beat the simplicity of programming a BTN for small problem sizes (and values of p).

5 Conclusion

An experimental study of integer sorting on multicores was undertaken using multithreading and multiprocessing programming approaches resulting in code that is portable and transportable and works without any modifications under three multithreading or multiprocessing libraries, Open MPI, MulticoreBSP, and BSPlib. We have implemented serial [7] and parallel radix-sort for various radixes and also some previously little explored or unexplored variants of bitonic-sort and odd-even transposition sort. Moreover we implemented two variants of random oversampling parallel sorting algorithms and made them to work in the context of integer sorting, as well as a deterministic regular oversampling parallel sorting algorithm. To the best of our knowledge this is the first time that so many diverse and varying structure and concept algorithms have been benchmarked against one another.

We have offered a series of observations obtained through this evaluation and presented in a systematic way. Some of those observations have been made previously, but some of them might not be valid any more for modern architectures. Moreover we have expressed the performance of some of our implementations in the context of the MBSP model [17]. We showed how one can use the model to compare the theoretical performance of the implementations involving SR4, PR4 and GSD. Several conclusions drawn through this theoretical comparison are in line with the experimental results we obtained. This would suggest that MBSP might have merit in studying the behavior of multicore and multi-memory hierarchy algorithms and thus be a useful and usable model. We have also highlighted why precise and accurate performance prediction might be difficult to achieve with MBSP or more complex and hierarchical models. Complex algorithms exhibit complex and difficult to precisely model memory interactions and patterns. Furthermore, users interact with memory through third-party libraries that facilitate parallel multithreading or multiprocessing programming. Modeling such libraries or their interactions with memory is next to impossible.

References

[1] K. Batcher. Sorting Networks and their applications. In *Proceedings of the AFIPS Spring Joint Computing Conference,* pp. 307-314, 1968.

[2] G. Baudet and D. Stevenson. Optimal sorting algorithms for parallel computers. IEEE Transactions on Computers, C-27(1):84-87, 1978.

[3] G. E. Blelloch, C. E. Leiserson, B. M. Maggs, C. G. Plaxton, S. J. Smith, and M. Zagha. A comparison of sorting algorithms for the connection machine CM-2. In Proc. of the Symposium on Parallel Algorithms and Architectures (SPAA '91), pp. 3-16, Hilton Head, SC, USA, July 21-24, ACM Press, 1991.

[4] B. Bramas. Fast Sorting Algorithms using AVX-512 on Intel Knights Landing. arXiv:1704.08579, 24 Apr 2017.

[5] D. Cederman and P. Tsingas. On sorting and load balancing on GPUs. In Proc. ACM SIGARCH Computer Architecture News, Vol. 36(5), Dec. 2008, pp 11-18, ACM NY, USA.

[6] Z. Cheng, K. Qi, L. Jun, and H. Yi-Ran. Thread-Level Parallel Algorithm for Sorting Integer Sequence on Multi-core Computers. In Proc. International Symposium on Parallel Architectures, Algorithms and Programming, Tianjin, China, Dec. 9-11, 2011, pp. 37-41, IEEE Press. DOI Bookmark: http://doi.ieeecomputersociety.org/10.1109/PAAP.2011.57

[7] T. H.Cormen, C. E. Leiserson, R. L. Rivest, and C. Stein. Introduction to Algorithms, Third Edition. The MIT Press, 2009.

[8] A. Chan and F. Dehne.and H. Zaboli. A note on coarse grained parallel integer sorting. Parallel Processing Letters, Vol. 9, No. 4, pp. 533-538, 1999.

[9] F. Dehne and H. Zaboli. Deterministic Sample sort for GPUs. Parallel Processing Letters, Vol. 22, No. 3, pp. 1250008-1 to 1250008-14, 2012.

[10] F. Dehne and H. Zaboli. Parallel Sorting for GPUs. In: Adamatzky A. (eds) Emergent Computation. Emergence, Complexity and Computation, vol 24., pp 293-302, Springer, 2017.

[11] W. D. Frazer and A. C. McKellar. Samplesort: A sampling approach to minimal storage tree sorting. *Journal of the ACM*, 17(3):496-507, 1970.

[12] Brian A. Garber, Dan Hoeflinger, Xiaoming Li, Maria Jesus Garzaran, and David Padua. Automatic Generation of a Parallel Sorting Algorithm. IEEE International Symposium on Parallel and Distributed Processing, 2008, 14-18 April 2008, p 1-5.

[13] A. V. Gerbessiotis and C. J. Siniolakis. Deterministic sorting and randomized median finding on the BSP model. In *Proceedings of the 8-th Annual ACM Symposium on Parallel Algorithms and Architectures*, pp. 223-232, Padua, Italy, June 1996.

[14] A. V. Gerbessiotis and C. J. Siniolakis. An Experimental Study of BSP Sorting Algorithms. In Proceedings of 6th Euromicro Workshop on Parallel and Distributed Processing, Madrid, Spain, January, IEEE Computer Society Press, 1998.

[15] A. V. Gerbessiotis and C. J. Siniolakis. Efficient deterministic sorting on the BSP model. Parallel Processing Letters, Vol 9 No 1 (1999), pp 69-79, World Scientific Publishing Company.

[16] A. V. Gerbessiotis and L. G. Valiant. Direct bulk-synchronous algorithms. *Journal of Parallel and Distributed Computing*, 22:251-267, Academic Press, 1994.

[17] A. V. Gerbessiotis. "Extending the BSP model for multi-core and out-of-core computing: MBSP", Parallel computing 41 (2015) 90-102.

[18] A. V. Gerbessiotis. `http://www.cs.njit.edu/~alexg/cluster/software.html`. July 2018.

[19] D. B. Skillicorn, J. M. D. Hill, and W. F. McColl. Questions and answers about BSP. Scientific Programming, 6 (1997), pp. 249-274.

[20] C. A. R. Hoare. Quicksort. *The Computer Journal*, 5:10-15, 1962.

[21] J. S. Huang and Y. C. Chow. Parallel sorting and data partitioning by sampling. *IEEE Computer Society's Seventh International Computer Software and Applications Conference*, pages 627–631, November 1983.

[22] H. Inoue, T. Moriyama, H. Komatsu and T. Nakatani. A high-performance sorting algorithm for multicore single-instruction multiple-data processors. Softw. Pract. Exper., 42: 753777. doi:10.1002/spe.1102, Wiley, 2012.

[23] M. F. Ionescu and K. E. Schauser. Optimizing parallel bitonic sort. In Proc. IEEE Parallel Processing Symposium, Geneva, Switzerland, IEEE, pp 303-309, 1997.

[24] Knuth D. E. *The Art of Computer Programming. Volume III: Sorting and Searching.* Addison-Wesley, Reading, 1973.

[25] D. Langr, P. Tvrdik, and I. Simecek. AQsort: Scalable Multi-Array In-Place Sorting with OpenMP. Scalable Computing: Practice and Experience, Vol 17(4), pp 369-391,SCPE, 2016.

[26] F. T. Leighton. *Introduction to Parallel Algorithms and Architectures: Arrays - Trees - Hypercubes.* Morgan Kaufmann, California, 1991.

[27] D. Nassimi and S. Sahni. Parallel permutation and sorting algorithms and a new generalized connection network. *Journal of the ACM*, 29:3:642:667, July 1982.

[28] A. Maus. A full parallel radix sorting algorithm for multicore processors. In Proc. Norsk Informatikkonferanse (NIK 2011), pp. 37-48, 2011.

[29] R.L. Graham, T.S. Woodall, J.M. Squyres. Open MPI: A Flexible High Performance MPI. In Proceedings, 6th Annual International Conference on Parallel Processing and Applied Mathematics, September 2005, Poznan, Poland, Springer Verlag Lecture Series in Computer Science, pp. 228-239, Lecture Notes in Computer Science, Vol. 3911, Springer.

[30] H. Peters, O. Schulz-Hildebrandt and N. Luttenberger. Fast in-place, comparison-based sorting with CUDA: a study with bitonic sort. Concurrency Computat.: Pract. Exper., 23: 681693, 2011. doi:10.1002/cpe.1686

[31] S. Rathi. Optimizing sorting algorithms using ubiquitous multi-core massively parallel GPGPU processors. In Proceedings 7th Int. Conference on Communication, Computing, and Vizualization, 2016, Procedia Computer Science 79, pp. 231-237, 2016.

[32] H. J. Reif and L. G. Valiant. A logarithmic time sort for linear size networks. *Journal of the ACM,* 34:60-76, January 1987.

[33] R. Reischuk. Probabilistic parallel algorithms for sorting and selection. *SIAM Journal on Computing,* 14(2):396-409, 1985.

[34] H. Shi and J. Schaeffer. Parallel sorting by regular sampling. *Journal of Parallel and Distributed Computing*, 14:362-372, 1992.

[35] L. G. Valiant. A bridging model for parallel computation. *Comm. of the ACM,* 33(8):103-111, August 1990.

[36] A. N. Yzelman, R. H. Bisseling, D. Roose, and K. Meerbergen. MulticoreBSP for C: a high-performance library for shared-memroy parallel programming. Technical report TW 624, KU Leuven, 2013. Also International Journal of Parallel Programming, Vol. 42(4), pp 619-642, August 2014, Springer.

[37] L. G. Valiant. A bridging model for multi-core computing. *Journal of Computer and System Sciences,* 77(1):154-166, 2011.

[38] S. S. Zaghloul, L. M. AlShehri, M. F. AlJouie, N. E. AlEissa, N. A. AlMogheerah. Analytical and experimental performance evaluation of parallel merge sort on multi-core systems. International Journal of Engineering and Computer Science, Vol 6 (6), pp. 21764-21773, June 2017.

[39] C. Zhong, Z. Qu, F. Yang, M. Yin, X. Li. Efficient and scalable parallel algorithm for sorting multisets on multi-core systems. Journal of Computers, Vol 7(1), pp. 30-41, IAP, January 2012.

Table 1. Time(sec) for SR4; Speedup for other on CONFIG1

Speedup on Intel Platform										
		OpenMPI			MulticoreBSP			BSPlib		
		8M	32M	128M	8M	32M	128M	8M	32M	128M
SR4	$p = 1$	0.250	1.160	5.290	0.250	1.160	5.290	0.250	1.160	5.290
PR4	$p = 4$	3.47	3.86	3.39	3.24	3.67	3.70	3.01	3.29	3.12
PR4	$p = 8$	5.68	6.82	7.00	5.81	6.55	7.18	5.81	5.57	6.31
PR4	$p = 16$	7.57	10.84	12.90	9.61	10.26	11.65	10.00	7.68	11.45
PR4	$p = 32$	4.38	9.28	15.88	11.36	11.95	14.14	10.00	12.47	16.58
PR2	$p = 4$	1.59	2.22	2.82	2.11	2.71	3.12	0.76	1.66	2.73
PR2	$p = 8$	1.52	2.63	4.30	3.08	4.56	5.31	0.62	1.45	3.65
PR2	$p = 16$	1.05	2.07	4.65	5.10	5.65	6.73	0.56	0.99	3.77
PR2	$p = 32$	0.44	1.10	4.59	5.81	6.13	7.45	0.46	0.89	3.33
BTN	$p = 4$	2.71	2.76	2.42	2.29	2.43	2.58	2.25	2.60	2.36
BTN	$p = 8$	3.67	3.86	3.67	2.97	3.38	3.77	2.87	3.50	3.85
BTN	$p = 16$	4.31	4.64	4.70	3.67	4.18	4.80	3.62	3.95	4.23
BTN	$p = 32$	3.12	3.07	4.05	3.33	3.53	4.35	3.33	3.58	4.54
OET	$p = 4$	2.57	2.61	2.27	1.89	1.99	2.13	1.98	2.20	2.06
OET	$p = 8$	2.90	3.12	3.03	2.19	2.43	2.73	2.19	2.54	2.80
OET	$p = 16$	2.52	2.85	3.37	2.57	2.76	2.99	2.42	2.47	2.74
OET	$p = 32$	1.63	1.59	1.94	1.87	2.09	2.44	1.60	1.68	2.24
GSD	$p = 4$	3.16	3.03	2.65	2.84	2.87	2.96	2.77	2.96	2.66
GSD	$p = 8$	5.55	5.37	4.62	4.71	5.00	5.20	4.31	3.42	5.06
GSD	$p = 16$	8.62	8.85	9.18	7.35	7.83	9.31	8.33	7.53	7.97
GSD	$p = 32$	10.0	9.13	11.23	9.61	7.29	10.70	10.41	10.84	12.53
GVR	$p = 4$	2.90	2.78	3.24	2.87	2.78	3.10	2.87	2.75	3.20
GVR	$p = 8$	5.00	5.13	5.63	4.80	5.00	5.76	4.31	4.42	5.54
GVR	$p = 16$	8.06	8.46	9.65	7.81	8.28	9.32	7.81	8.22	9.34
GVR	$p = 32$	8.62	9.66	11.91	8.62	9.13	11.52	9.61	10.54	12.13
GER	$p = 4$	3.28	3.23	2.81	2.94	3.01	3.11	2.74	3.05	2.76
GER	$p = 8$	5.00	5.34	4.89	4.90	4.91	5.55	4.16	4.01	5.35
GER	$p = 16$	8.62	8.72	8.74	7.57	7.58	9.21	8.33	7.68	7.82
GER	$p = 32$	9.61	9.35	11.96	10.86	7.43	9.94	9.61	10.94	12.83

Table 2. Time(sec) for SR4; Speedup for other on CONFIG2

Speedup on Intel Platform										
		OpenMPI			MulticoreBSP			BSPlib		
		8M	32M	128M	8M	32M	128M	8M	32M	128M
SR4	$p = 1$	0.340	1.360	7.300	0.340	1.360	7.300	0.340	1.360	7.300
PR4	$p = 4$	2.31	2.46	3.25	2.32	2.29	3.10	1.79	1.84	2.45
PR4	$p = 8$	3.90	4.01	5.32	3.73	3.56	4.92	3.11	2.99	3.91
PR4	$p = 16$	4.41	5.48	7.56	4.59	4.75	6.59	4.72	4.30	5.82
PR4	$p = 32$	4.53	5.25	7.79	6.66	5.35	7.65	4.78	4.57	6.50
PR2	$p = 4$	1.39	1.78	2.53	2.37	2.93	4.36	0.67	1.75	3.61
PR2	$p = 8$	1.21	1.85	2.81	3.57	4.40	6.57	0.47	1.56	4.49
PR2	$p = 16$	0.85	1.60	2.84	4.30	4.54	6.41	0.29	1.04	4.01
PR2	$p = 32$	0.54	1.10	2.27	4.47	5.31	7.94	0.18	0.64	2.86
BTN	$p = 4$	1.89	1.85	2.46	2.09	1.97	2.69	1.87	1.85	2.36
BTN	$p = 8$	2.44	2.21	2.84	2.22	2.24	2.94	2.31	2.09	2.68
BTN	$p = 16$	2.06	1.73	2.27	1.78	1.87	2.47	1.97	1.67	2.20
BTN	$p = 32$	1.49	1.20	1.56	1.45	1.19	1.60	1.45	1.16	1.52
OET	$p = 4$	1.67	1.63	2.20	1.71	1.68	2.23	1.38	1.38	1.76
OET	$p = 8$	1.98	1.82	2.39	2.03	1.97	2.62	1.57	1.47	1.89
OET	$p = 16$	1.25	1.08	1.42	1.25	1.36	1.79	1.23	1.04	1.37
OET	$p = 32$	0.63	0.53	0.69	0.63	0.59	0.81	0.66	0.54	0.72
GSD	$p = 4$	2.65	2.47	3.16	2.51	2.40	3.14	2.37	2.28	2.87
GSD	$p = 8$	5.31	4.44	5.16	4.30	3.86	4.79	4.59	4.04	4.67
GSD	$p = 16$	8.50	6.15	7.23	5.48	4.90	6.30	7.39	5.69	6.72
GSD	$p = 32$	12.14	6.80	6.93	7.90	4.54	6.38	10.62	6.26	6.64
GVR	$p = 4$	2.26	2.15	3.03	2.41	2.14	2.97	2.34	2.29	2.76
GVR	$p = 8$	4.59	4.04	5.40	3.95	3.76	4.97	4.30	3.89	4.77
GVR	$p = 16$	7.39	6.21	7.92	5.66	5.59	7.08	6.80	5.86	7.65
GVR	$p = 32$	9.71	7.39	9.69	9.18	6.41	9.31	8.94	7.01	8.93
GER	$p = 4$	2.74	2.63	3.36	2.59	2.46	3.31	2.55	2.41	3.04
GER	$p = 8$	4.85	4.31	5.50	4.35	3.82	4.95	4.35	4.04	4.93
GER	$p = 16$	8.50	6.15	7.13	5.76	4.78	6.29	7.55	5.69	6.66
GER	$p = 32$	12.59	6.86	7.22	11.72	4.72	6.31	10.62	6.38	6.73

Table 3. Time(sec) for SR4; Speedup for other on CONFIG3

Speedup on Intel Platform										
		OpenMPI			MulticoreBSP			BSPlib		
		8M	32M	128M	8M	32M	128M	8M	32M	128M
SR4	$p = 1$	0.241	1.056	4.200	0.241	1.056	4.200	0.241	1.056	4.200
PR4	$p = 4$	3.21	3.41	3.36	3.05	3.25	3.20	2.53	2.54	2.63
PR4	$p = 8$	5.23	6.10	6.14	5.47	5.67	4.46	4.08	4.73	4.62
PR4	$p = 16$	7.30	9.96	10.16	8.92	8.87	8.95	7.53	7.23	7.54
PR4	$p = 32$	4.54	10.66	11.86	11.47	11.00	11.32	8.92	10.77	11.32
PR2	$p = 4$	1.46	1.87	1.91	1.94	2.30	2.32	0.54	1.35	2.00
PR2	$p = 8$	1.44	2.35	2.65	3.08	3.89	3.80	0.41	1.34	2.66
PR2	$p = 16$	1.00	1.83	2.88	4.46	5.00	5.10	0.31	1.06	2.62
PR2	$p = 32$	0.42	1.07	2.03	5.60	5.70	6.00	0.18	0.74	1.86
BTN	$p = 4$	2.73	2.61	2.53	2.80	2.62	2.59	2.29	2.31	2.22
BTN	$p = 8$	3.76	3.71	3.62	3.70	3.71	3.16	2.90	3.15	2.92
BTN	$p = 16$	4.30	4.31	4.28	4.08	4.24	4.19	3.25	3.79	3.58
BTN	$p = 32$	2.43	3.79	3.68	3.59	3.56	3.84	3.12	3.23	3.08
OET	$p = 4$	2.61	2.46	2.40	2.48	2.39	2.33	1.83	1.91	1.85
OET	$p = 8$	2.90	2.97	2.93	3.05	3.15	2.96	2.21	2.34	2.20
OET	$p = 16$	2.36	2.50	2.56	3.12	3.36	3.12	2.36	2.57	2.41
OET	$p = 32$	1.56	2.08	1.84	2.13	2.26	2.36	1.52	1.48	1.38
GSD	$p = 4$	3.12	2.84	2.73	2.93	2.65	2.69	2.59	2.56	2.44
GSD	$p = 8$	5.35	5.00	4.45	4.91	4.61	4.00	4.15	4.45	3.77
GSD	$p = 16$	8.31	8.00	8.04	6.88	6.72	6.38	5.60	7.23	7.79
GSD	$p = 32$	9.64	10.25	10.16	9.26	5.61	7.48	9.26	10.15	7.25
GVR	$p = 4$	2.90	2.65	2.92	3.17	2.77	2.87	2.56	2.35	2.70
GVR	$p = 8$	5.02	4.82	4.74	5.12	4.84	4.52	4.08	4.47	4.42
GVR	$p = 16$	7.53	7.59	7.52	7.53	7.23	6.22	5.23	7.13	7.17
GVR	$p = 32$	8.31	9.26	9.48	8.60	8.38	8.30	8.92	9.42	9.52
GER	$p = 4$	3.21	2.97	2.87	3.08	2.89	2.82	2.70	2.65	2.58
GER	$p = 8$	4.82	4.93	4.74	5.02	4.63	4.32	3.88	4.41	3.92
GER	$p = 16$	8.31	7.82	7.85	7.30	6.17	6.26	6.34	7.23	7.48
GER	$p = 32$	9.64	10.15	10.37	10.04	5.67	7.16	9.26	10.15	9.97

Table 4. Time(sec) for SR4; Speedup for other on CONFIG4

Speedup on Intel Platform										
		OpenMPI			MulticoreBSP			BSPlib		
		8M	32M	128M	8M	32M	128M	8M	32M	128M
SR4	$p = 1$	0.054	0.224	0.840	0.054	0.224	0.840	0.054	0.224	0.840
PR4	$p = 2$	1.35	1.34	1.30	1.01	1.01	1.03	1.28	1.28	1.23
PR4	$p = 4$	1.38	1.86	1.33	1.22	1.20	1.15	1.63	1.70	1.54
PR4	$p = 8$	1.68	1.83	1.67	1.20	1.22	1.10	1.63	1.72	1.56
PR2	$p = 2$	0.69	0.80	0.78	0.80	0.82	0.82	0.37	0.67	0.79
PR2	$p = 4$	0.53	0.79	0.67	0.80	0.85	0.81	0.30	0.64	0.82
PR2	$p = 8$	0.34	0.50	0.50	0.56	0.62	0.59	0.18	0.43	0.57
BTN	$p = 2$	1.08	1.10	1.03	1.03	1.04	0.97	1.08	1.044	0.95
BTN	$p = 4$	0.85	1.05	0.79	0.93	0.93	0.95	0.98	1.00	0.91
BTN	$p = 8$	0.70	0.72	0.66	0.60	0.62	0.56	0.68	0.70	0.63
OET	$p = 2$	1.10	1.12	1.05	1.08	1.04	0.98	1.14	1.10	1.03
OET	$p = 4$	0.83	1.05	0.80	0.96	0.95	0.87	1.01	1.03	0.93
OET	$p = 8$	0.65	0.70	0.63	0.59	0.62	0.56	0.65	0.67	0.61
GSD	$p = 2$	1.14	1.15	1.08	1.28	1.24	1.12	1.35	1.29	1.22
GSD	$p = 4$	1.12	1.35	0.97	1.54	1.40	1.33	1.58	1.58	1.42
GSD	$p = 8$	1.31	1.33	1.16	1.28	1.37	1.17	1.42	1.43	1.22
GVR	$p = 2$	0.96	0.97	0.92	1.14	0.99	0.97	1.22	1.15	1.10
GVR	$p = 4$	0.91	1.19	0.86	1.58	1.53	1.35	1.54	1.58	1.40
GVR	$p = 8$	1.14	1.19	1.06	1.42	1.48	1.27	1.50	1.50	1.32
GER	$p = 2$	1.20	1.28	1.12	1.31	1.15	1.14	1.38	1.31	1.23
GER	$p = 4$	1.08	1.43	1.04	1.54	1.56	1.35	1.63	1.63	1.42
GER	$p = 8$	1.31	1.36	1.21	1.28	1.38	1.23	1.38	1.42	1.28

Table 5. Small problem size experiments on CONFIG3

Time in microseconds										
		OpenMPI			MulticoreBSP			BSPlib		
		8192	32768	131072	8192	32768	131072	8192	32768	131072
SR4	$p = 1$	109	483	2076	109	483	2076	109	483	2076
PR4	$p = 4$	678	855	1400	282	397	886	829	209	2571
PR4	$p = 16$	1404	1218	1933	633	655	987	417	482	4356
PR4	$p = 32$	3338	8225	6818	1259	1307	1512	516	6807	6067
BTN	$p = 4$	102	268	896	72	274	1105	86	298	944
BTN	$p = 16$	254	362	1062	151	236	699	176	304	731
BTN	$p = 32$	972	1990	2608	290	382	816	401	426	904
GSD	$p = 4$	187	338	855	93	249	908	117	261	744
GSD	$p = 16$	406	408	909	181	237	484	416	495	645
GSD	$p = 32$	2030	2347	2589	348	374	619	1120	1029	1184
GVR	$p = 4$	237	424	1055	207	425	1248	135	339	938
GVR	$p = 16$	541	534	1075	496	665	1044	373	463	672
GVR	$p = 32$	1248	2376	2620	988	1252	1762	987	909	1071
GER	$p = 4$	211	373	862	138	293	965	116	286	768
GER	$p = 16$	492	498	1006	464	594	890	411	531	654
GER	$p = 32$	1207	2455	2586	1017	1216	1646	1080	1030	1172